What is claimed is:

1. A manufacturing method of a semiconductor integrated circuit device having a plurality of first MISFETs in a first region and a plurality of second MISFETs in a second region, comprising the steps of:

(a) forming a first insulating film between two adjacent regions of said first MISFET forming regions in said first region and said second MISFET forming regions in said second region,

(b) forming a second insulating film over a surface of said semiconductor substrate between said first insulating films in each of said first and second regions,

(c) depositing a third insulating film over said second insulating film,

(d) forming a first conductive film over said third insulating film in said second region,

(e) forming, after removal of said third and second insulating films from said first region, a fourth insulating film over the surface of said semiconductor substrate in said first region, and

(f) forming a second conductive film over said fourth insulating film,

(g) wherein said third insulating film remains over said first insulating film in said second region.

2. A manufacturing method of a semiconductor

integrated circuit device according to claim 1, wherein said first insulating film is an oxide film formed by thermal oxidation.

3. A manufacturing method of a semiconductor integrated circuit device according to claim 1, wherein said third insulating film is formed by CVD.

4. A manufacturing method of a semiconductor integrated circuit device according to claim 1, wherein an etching rate of said third insulating film is greater than that of said first insulating film.

5. A manufacturing method of a semiconductor integrated circuit device according to claim 1, wherein said third insulating film is thicker than said second insulating film.

6. A manufacturing method of a semiconductor integrated circuit device according to claim 1, wherein said first and second conductive films are each made of polysilicon.

7. A manufacturing method of a semiconductor integrated circuit device according to claim 1, wherein the third insulating film over said first insulating film is formed so that end portions of said third insulating film is positioned on said first insulating film.

8. A manufacturing method of a semiconductor integrated circuit device according to claim 1, wherein

said first insulating film forming step comprises forming a groove in said semiconductor substrate and forming an oxide film within said groove.

9. A manufacturing method of a semiconductor integrated circuit device according to claim 1, wherein the first insulating film in said first region is narrower than the first insulating film in said second region.

10. A manufacturing method of a semiconductor integrated circuit device according to claim 1, wherein said first insulating film is also formed at both ends of said first conductive film forming region.

11. A manufacturing method of a semiconductor integrated circuit device according to claim 1, wherein said first insulating film is also formed at both ends of the first conductive film forming region within said second region, and

said manufacturing method further comprises forming first semiconductor regions in the semiconductor substrate below the first insulating film formed at both ends of said first conductive film forming region, and

forming second semiconductor regions within said first semiconductor regions but outside of the first insulating film formed at both ends of the first conductive film forming region.

12. A manufacturing method of a semiconductor

integrated circuit device according to claim 1, wherein the impurity concentration of said first semiconductor regions is lower than that of said second semiconductor regions.

13. A manufacturing method of a semiconductor integrated circuit device having a plurality of first MISFETs in a first region of a semiconductor substrate and a plurality of second MISFETs in a second region, comprising the steps of:

(a) forming a first insulating film between two adjacent regions of said first MISFET forming regions in said first region and said second MISFET forming regions in said second region,

(b) forming a second insulating film on a surface of the semiconductor substrate between said first insulating films in said first and second regions,

(c) depositing a third insulating film over said second insulating film,

(d) removing said third insulating film from said first region without removing said third insulating film over said first insulating film in said second region,

(e) depositing a first conductive film in said first and second regions on said semiconductor substrate,

(f) removing said first conductive film from said first region and a portion of said first conductive film from said second region,

(g) forming a fourth insulating film on the surface of said semiconductor substrate in said first region, and

(h) forming a second conductive film in said first region.

14. A manufacturing method of a semiconductor integrated circuit device according to claim 13, wherein said first insulating film is an oxide film formed by thermal oxidation.

15. A manufacturing method of a semiconductor integrated circuit device according to claim 13, wherein said third insulating film is formed by CVD.

16. A manufacturing method of a semiconductor integrated circuit device according to claim 13, wherein an etching rate of said third insulating film is greater than that of said first insulating film.

17. A manufacturing method of a semiconductor integrated circuit device according to claim 13, further comprising, between said step (d) and said step (e), heat treating said third insulating film.

18. A manufacturing method of a semiconductor integrated circuit device according to claim 17, wherein said heat treatment is conducted at 900°C or greater.

19. A manufacturing method of a semiconductor integrated circuit device according to claim 17, wherein said heat treatment is conducted at 1000°C or greater.

20. A manufacturing method of a semiconductor integrated circuit device according to claim 13, wherein said third insulating film is thicker than said second insulating film.

21. A manufacturing method of a semiconductor integrated circuit device according to claim 13, wherein said first and second conductive films are each made of polysilicon.

22. A manufacturing method of a semiconductor integrated circuit device according to claim 13, wherein said first insulating film forming step comprises forming a groove in said semiconductor substrate and forming an oxide film in said groove.

23. A manufacturing method of a semiconductor integrated circuit device according to claim 13, wherein the first insulating film in said first region is narrower than the first insulating film in said second region.

24. A manufacturing method of a semiconductor integrated circuit device having, in a first region of a semiconductor substrate, a plurality of first MISFETs equipped with a gate electrode and source·drain regions and, in a second region, a plurality of second MISFETs equipped with a gate electrode and source·drain regions, comprising the steps of:

(a) forming a first insulating film between two

adjacent regions of said first MISFET forming regions in said first region and said second MISFET forming regions in said second region,

(b) forming a first semiconductor region in said first region and a second semiconductor region in said second region,

(c) forming a second insulating film on a surface of said semiconductor substrate between said first insulating films,

(d) depositing a third insulating film over said second insulating film,

(e) removing said second and third insulating films in said first region, and removing a portion of the second and third insulating films over said second semiconductor region in said second region, thereby forming a first opening,

(f) forming a first conductive film to be a gate electrode of said second MISFET over said third insulating film in said second region of said semiconductor substrate,

(g) forming a fourth insulating film over the surface of the semiconductor substrate in said first region,

(h) forming a second conductive film to be a gate electrode of said first MISFET over said fourth insulating film in said first region, and

(i) introducing an impurity on the surface of said

semiconductor substrate in order to form third semiconductor regions having a conductivity type contrary to that of said first semiconductor regions on both sides of said gate electrode of said first region and a fourth semiconductor region having the same conductivity type as that of said second semiconductor regions below said first opening in said second region.

25. A manufacturing method of a semiconductor integrated circuit device according to claim 24, wherein said third insulating film constituting said first opening portion has side walls above said first insulating film.

26. A manufacturing method of a semiconductor integrated circuit device according to claim 24, wherein a fixed voltage is applied to said fourth semiconductor region.

27. A manufacturing method of a semiconductor integrated circuit device according to claim 24, wherein the first insulating film in said first region is narrower than the first insulating film in said second region.

28. A manufacturing method of a semiconductor integrated circuit device having a first MISFET in a first region of a semiconductor substrate and a second MISFET in a second region, comprising the steps of:

(a) forming a first insulating film in said first and second regions,

(b) depositing a first conductive film over said first insulating film in said first and second regions,

(c) removing the first insulating film and the first conductive film in said first region,

(d) forming a second insulating film in said first region over said semiconductor substrate,

(e) depositing a second conductive film in said first and second regions, and

(f) implanting an impurity to said first and second regions downward from a position above said second conductive film at an energy permitting the impurity to reach the substrate in said first region.

29. A manufacturing method of a semiconductor integrated circuit device according to claim 28, further comprising the steps of:

(g) depositing a third conductive film over the second conductive film in each of said first and second regions, and

(h) removing a portion of said second and third conductive films in said first region, forming a gate electrode of said first MISFET comprised of the second and third conductive films and removing said second and third conductive films from said second region.

30. A manufacturing method of a semiconductor integrated circuit device according to claim 28, further

comprising the steps of:

(g) depositing a third conductive film over the second conductive film in each of said first and second regions,

(h) removing a portion of said second and third conductive films in said first region, forming a gate electrode of said first MISFET comprised of the second and third conductive films and removing the second and third conductive films from said second region, and

(i) removing a portion of said first conductive film from said second region and forming a gate electrode of said second MISFET.

31. A manufacturing method of a semiconductor integrated circuit device according to claim 28, which further comprising the step of:

(g) forming a fourth conductive film over said semiconductor substrate within said first region.

32. A manufacturing method of a semiconductor integrated circuit device according to claim 28, wherein implantation of the impurity stops at said first conductive film and the impurity does not reach said first insulating film.

33. A manufacturing method of a semiconductor integrated circuit device according to claim 28, wherein implantation of the impurity stops at said first conductive film and the impurity does not reach said semiconductor

substrate in said second region.

34. A manufacturing method of a semiconductor integrated circuit device according to claim 28, wherein said first conductive film is thicker than said second conductive film.

35. A manufacturing method of a semiconductor integrated circuit device according to claim 28, further comprising, between the step (d) and the step (e), heating in a nitrogen-containing atmosphere.

36. A manufacturing method of a semiconductor integrated circuit device having a plurality of first MISFETs in a first region of a semiconductor substrate and a plurality of second MISFETs in a second region, comprising the steps of:

(a) forming a first insulating film between two adjacent regions of said first MISFET forming regions in said first region and said second MISFET forming regions in said second regions,

(b) forming a second insulating film over a surface of said semiconductor substrate between said first insulating films,

(c) depositing a third insulating film over said second insulating film in each of said first and second regions,

(d) removing said third insulating film from said

first region,

(e) forming a first conductive film in said second region,

(f) exposing the surface of the semiconductor substrate in said first region while covering said third insulating film in said second region with said first conductive film and forming a fourth insulating film, and

(g) forming a second conductive film over the fourth insulating film in said first region.

37. A manufacturing method of a semiconductor integrated circuit device according to claim 36 further having a third region, comprising the steps of:

(a) forming the first insulating film in said third region,

(b) forming the first conductive film over said first insulating film in said third region,

(c) forming a fifth insulating film over said first conductive film in said third region, and

(d) forming the second conductive film over the fifth insulating film in said third region.

38. A manufacturing method of a semiconductor integrated circuit device according to claim 37, wherein said first and second conductive films and said fifth insulating film constitute a capacitative element.

39. A manufacturing method of a semiconductor

integrated circuit device according to claim 36, wherein the first insulating film in said first region is narrower than the first insulating film in said second region.

40. A semiconductor integrated circuit device having a plurality of first MISFETs in a first region of a semiconductor substrate and a plurality of second MISFETs in a second region, comprising the steps of:

(a) a first insulating film lying between two adjacent regions of said first MISFET forming regions in said first region and said second MISFET forming regions in said second region,

(b) a second insulating film formed over a surface of said semiconductor substrate between said first insulating films in said second region,

(c) a third insulating film formed over said first insulating film and said second insulating film in said second region,

(d) a first conductive film over said third insulating film in said second region,

(e) a fourth insulating film formed over the surface of said semiconductor substrate in said first region, and

(f) a second conductive film formed over said fourth insulating film in said first region.

41. A semiconductor integrated circuit device according to claim 40, wherein said first insulating film

is thicker than any one of said second, third and fourth insulating films.

42. A semiconductor integrated circuit device according to claim 40, wherein the total thickness of said second and third insulating films is greater than the thickness of said fourth insulating film.

43. A semiconductor integrated circuit device having a plurality of first MISFETS on a semiconductor substrate, comprising the steps of:

(a) first insulating films each formed over a surface of said semiconductor substrate to cover each of said first MISFETs,

(b) a second insulating film formed over the surface of said semiconductor substrate between said first insulating films,

(c) a third insulating film formed over said second insulating film, and

(d) a first conductive film formed over said third insulating film,

(e) wherein said third insulating film exists over said first insulating film.

44. A semiconductor integrated circuit device according to claim 43, wherein said first insulating film is thicker than said second or third insulating film.

45. A semiconductor integrated circuit device

according to claim 43, wherein said third insulating film existing over said first insulating film has an end portion thereof over said first insulating film.

46. A semiconductor integrated circuit device according to claim 43 further having a second MISFET, comprising:

(a) a second insulating film formed over the surface of said semiconductor substrate between said first insulating films in said second MISFET region, and

(b) said first conductive film formed over said second insulating film.

47. A semiconductor integrated circuit device according to claim 43, wherein the first insulating film in said first region is narrower than the first insulating film in said second region.

48. A semiconductor integrated circuit device having a plurality of first MISFETs in a first region of a semiconductor substragte and a plurality of second MISFETs in a second region, comprising:

(a) first insulating films each formed over the surface of said semiconductor substrate between two adjacent regions of said first MISFET forming regions in said first region and said second MISFET forming regions in said second region,

(b) a first semiconductor region of a first

conductivity type formed in said semiconductor substrate in said first region and a second semiconductor region of a second conductivity type contrary to that of the first conductivity type formed in said semiconductor substrate in said second region,

(c) a second insulating film formed over the surface of said semiconductor substrate between said first insulating films in said second semiconductor region,

(d) a third insulating film having a first opening portion on the second semiconductor region in said second region and being formed over said first and second insulating films,

(e) a first conductive film formed over said third insulating film in said second semiconductor region,

(f) a fourth insulating film formed over the surface of said semiconductor substrate between said first insulating films in said first semiconductor region,

(g) a second conductive film formed over said fourth insulating film in said first semiconductor region,

(h) third semiconductor regions of the second conductivity type formed in said first semiconductor regions at both ends of said second conductive film, and

(i) a fourth semiconductor region of the second conductivity type formed below said first opening portion and in said second semiconductor region.

49. A semiconductor integrated circuit device according to claim 48, wherein end portions of said third insulating film constituting said first opening portion are more distant from said fourth semiconductor region than the end portions of said first insulating film on the side contiguous to said fourth semiconductor region.

50. A semiconductor integrated circuit device according to claim 48, wherein said second and fourth insulating films are oxide films formed by thermal oxidation.

51. A semiconductor integrated circuit device according to claim 48, wherein said third insulating film is formed by CVD.

52. A semiconductor integrated circuit device according to claim 48, wherein said third semiconductor region has substantially the same depth as that of said fourth semiconductor region.

53. A semiconductor integrated circuit device having a plurality of first MISFETs in a first region of a semiconductor substrate and a plurality of second MISFETs in a second region, comprising:

(a) a first insulating film formed between two adjacent regions of said first MISFET forming regions in said first region and said second MISFET forming regions in said second region,

(b) a first semiconductor region in said semiconductor substrate in said first region and a second semiconductor region in said semiconductor substrate in said second region,

(c) a second insulating film between said first insulating films in said first and second regions over said semiconductor substrate,

(d) a third insulating film having a first opening over the second semiconductor region in said second region,

(e) said third insulating film lying over said second insulating film in said second region,

(f) a first conductive film over said second insulating film in said first region and said first conductive film over said third insulating film in the second region,

(g) said third insulating film lying below said first conductive film in said second region, and

(h) third semiconductor regions of a conductivity type contrary to that of said first semiconductor region on both ends of said first conductive film in said first region and a fourth semiconductor region of the same conductivity type as that of the second semiconductor region below said first opening in said second region.

54. A semiconductor integrated circuit device according to claim 53, wherein end portions of said third

insulating film on a side contiguous to said first opening is more distant from said fourth semiconductor region than end portions of said first insulating film contiguous to said fourth semiconductor region.

55. A semiconductor integrated circuit device according to claim 53, wherein said first insulating film is an oxide film formed by thermal oxidation.

56. A semiconductor integrated circuit device according to claim 53, wherein said third insulating film is an oxide film formed by CVD.

57. A semiconductor integrated circuit device according to claim 53, wherein said first conductive film is made of polysilicon.

58. A semiconductor integrated circuit device having a plurality of first MISFETs in a first region of a semiconductor substrate and a plurality of second MISFETs in a second region, comprising:

(a) a first insulating film lying between two adjacent regions of said first MISFET forming regions in said first region and said second MISFET forming regions in said second region,

(b) a second insulating film formed over a surface of said semiconductor substrate between said first insulating films in said second region,

(c) a third insulating film formed in said second

region,

(d) a first conductive film lying over said third insulating film in said second region,

(e) a fourth insulating film formed on the surface of said semiconductor substrate between said first insulating films in said first region, and

(f) a second conductive film formed over said fourth insulating film in said first region.

59. A manufacturing method of a semiconductor integrated circuit device having a plurality of first MISFETs in a first region of a semiconductor substrate and a plurality of second MISFETs in a second region, comprising the steps of:

(a) forming a first insulating film over a surface of the semiconductor substrate in said first and second regions,

(b) depositing a second insulating film over said first insulating film in said first and second regions,

(c) forming a first conductive film over said second insulating film in said second region,

(d) exposing the surface of the semiconductor substrate in said first region while covering said second insulating film in said second region with said first conductive film, and forming a third insulating film, and

(e) forming a second conductive film over the third

insulating film in said first region.

60. A manufacturing method of a semiconductor integrated circuit device having a plurality of first MISFETs in a first region of a semiconductor substrate and a plurality of second MISFETs in a second region, comprising the steps of:

(a) forming a first insulating film made of a thermally oxidized film on a surface of the semiconductor substrate in said first and second regions,

(b) depositing a second insulating film over said first insulating film in said first and second regions,

(c) forming a first conductive film over said second insulating film in said second region,

(d) exposing the surface of the semiconductor substrate in said first region while covering said second insulating film in said second region with said first conductive film, and forming a third insulating film made of a thermally oxidized film, and

(e) forming a second conductive film over the third insulating film in said first region.